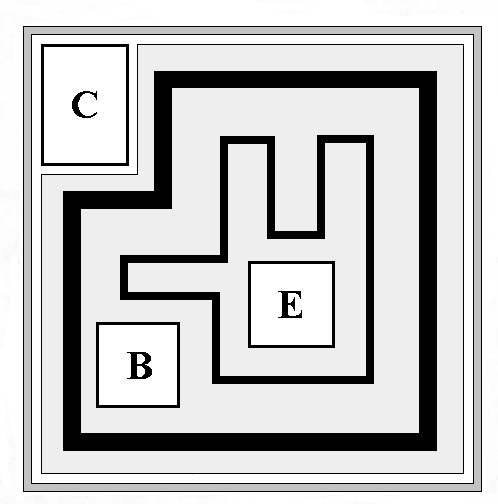
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.024”**



**.024”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004” min.**

**Backside Potential: Collector**

**Mask Ref: JSA**

**APPROVED BY: DK DIE SIZE .024” X .024” DATE: 9/7/21**

**MFG: ALLEGRO/SPRAGUE THICKNESS .010” P/N: 2N2907A**

**DG 10.1.2**

#### Rev B, 7/1